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Costly Controversial ESD Myths

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    - Current Scanning
    - ESD susceptibility scanning (for soft failures)
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Customer Base Examples

Outline – Costly Controversial ESD Myths

1. Myth: S20.20 Is Sufficient For Class 0 Technologies
2. Myth: HBM Failures Dominate ESD Failures
3. Myth: Circuit Boards are Less Sensitive to ESD than Devices
4. Myth: ESD is a Low Level Contributor to Device Failures
5. Myth: Airflow Causes Charging
6. Myth: Metalized Shielding Layers Are Essential
7. Myth: MM Is A Valid Simulation Related To Machines
8. Myth: Humidity Control is Essential for ESD
9. Myth: Fieldmeters Make Accurate Measurements on Machines
10. Myth: Ionization is Sufficient for Class 0 Applications
11. Myth: Latency Failures Comprise 90% of ESD Failures

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Examples:
Unnecessary Expenses Triggered by Controversial Myths

- **Unnecessary Gloves - $30,000/yr.**
- **Excessive Shielding:**
  - **Packaging Costs - $400,000/yr.**
  - **Packaging Costs - $140,000/yr.**
  - **Packaging Costs - $100,000/yr.**
- **Excessive Ionization - $100,000/Site**
- **CDM ESD Failures Unresolved - $240,000/yr.**
  - **Implemented Only S20.20 Procedures**
- **Overreaction to MM Data - $85,000**
- **Incorrect Class 0 Controls - $6 M**
- **Humidity Controls - $175,000/yr.**

Note: Overkill Expenses are Avoidable with Sound Technical Advice!

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Myth #1:

S20.20 Is Sufficient For Class 0 Technologies

Truth:
S20.20 Needs to be Customized to Include CDM, CBE, CDE, and Class 0

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"Class 0" Terms Used in this Tutorial

- Class 0
  - Blanket term used to refer to devices with thresholds less than 250 volts HBM or CDM (i.e., Class OA or OB)
- Class 0B
  - Withstand Voltage greater than/equal to 125 volts and less than 250 volts HBM or CDM
- Class 0A
  - Withstand Voltages Less than 125 volts HBM or CDM
- Class "000"
  - Withstand voltage Less than 50 volts

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Industry Standards Lag Technology 10 to 15 years

Best Industry Manufacturing Standard

2014 ANSI/ESDA S20.20

Scope:

HBM > 100V

CDM > 200 V

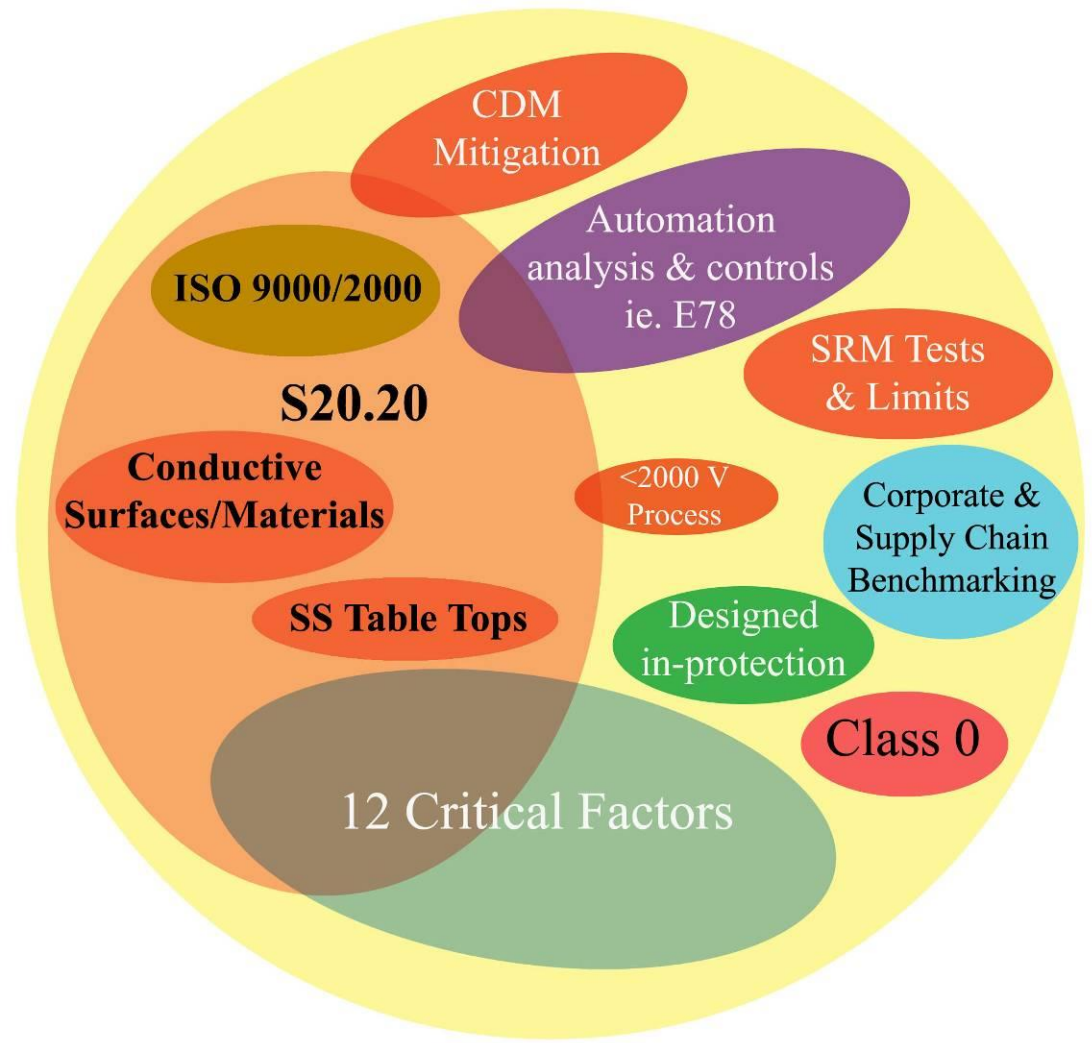
Metal Objects > 35 V

However:

- **No CDM SRM Requirements**
- **Metal at 35 V is High Risk**

Thus:

S20.20 Customization is <u>Essential</u> for : Class 0, CBE, CDE & CDM



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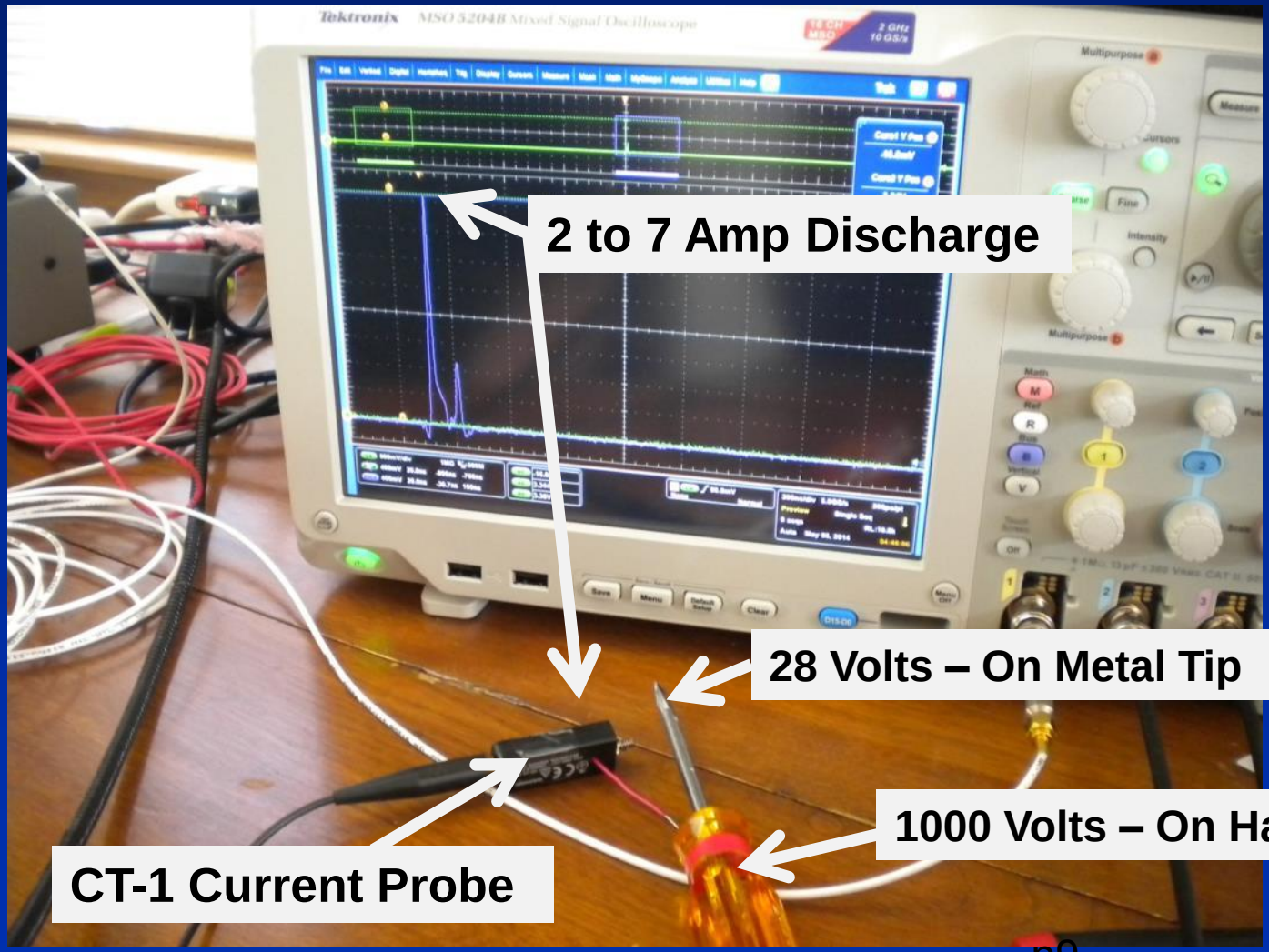
Isolated Conductor Example:
Charged Screwdriver (28 Volts)
Root Cause of CDM Damage to Devices on Boards



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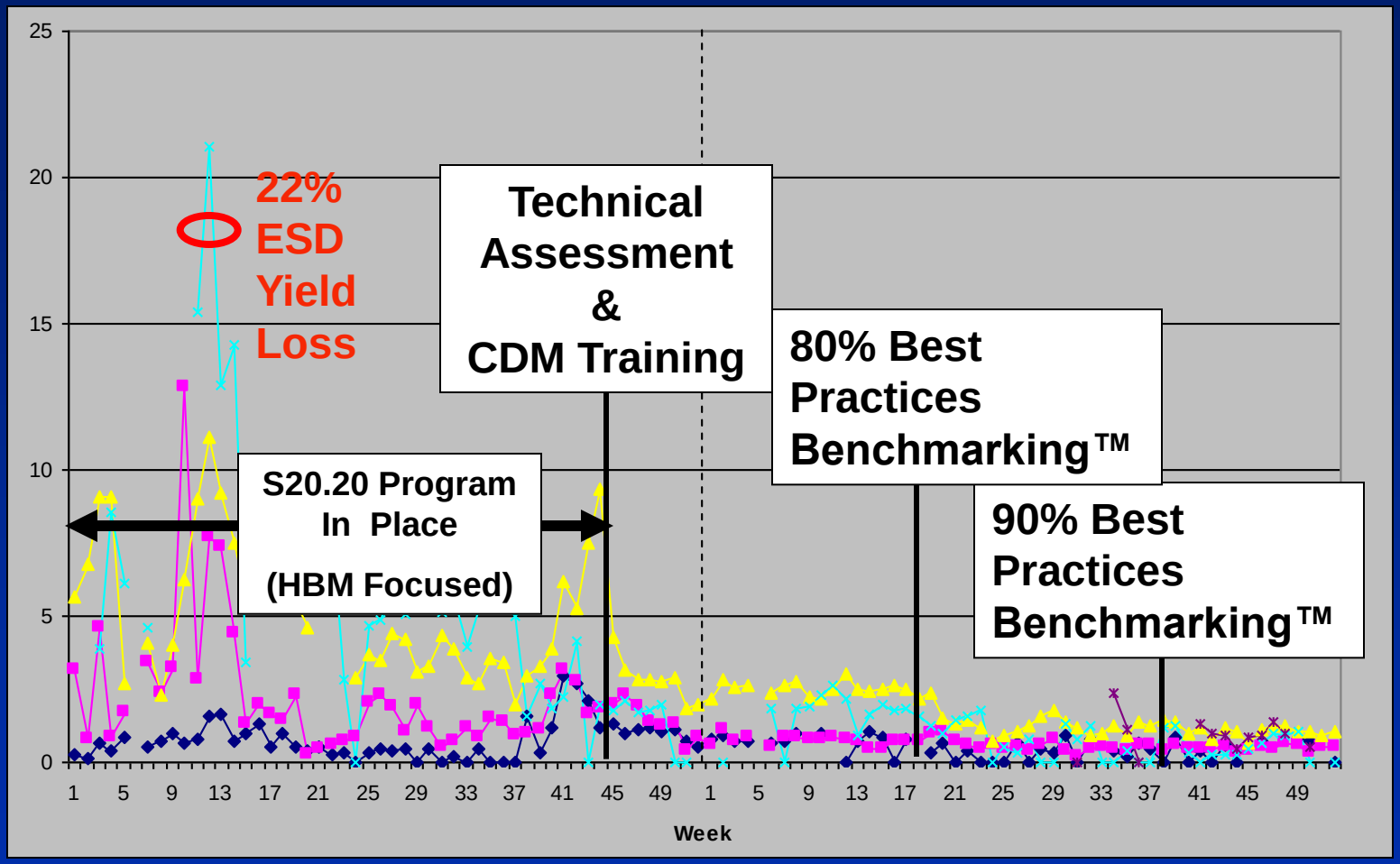
Class 00 Benchmarking Case Study Corresponding Yield Improvements



Note: Courtesy Herald Datanetics ltd. - 1st Class 0 Certified Manufacturing Operation http://www.dangelmayer.com/class-0-certification.php **Each data point is confirmed ESD damage during production (typically 65 volt CDM/HBM ESD sensitivity) and different colors represent different products.**

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Myth #2:
HBM Dominates ESD Failures

Truth:
Laboratory Failure Analysis Data From Major IC Suppliers (TI, ADI, Intel etc.) Indicates the Vast Majority of ESD Device Failures are CDM in Nature

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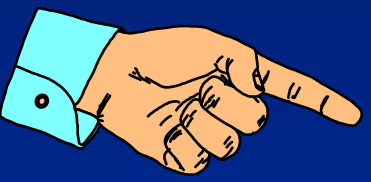
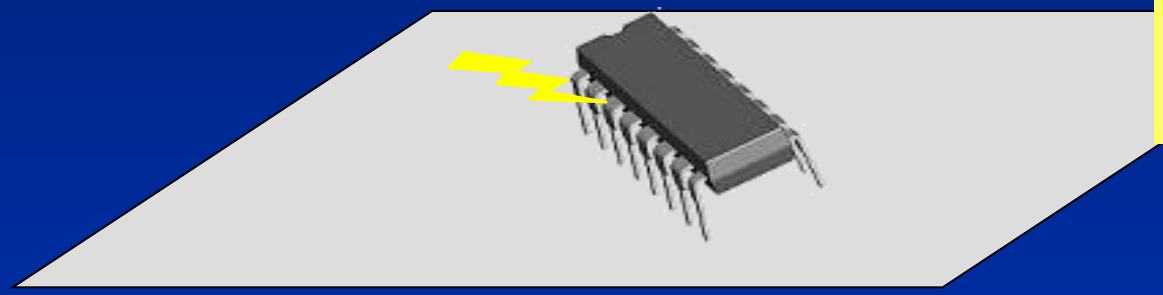
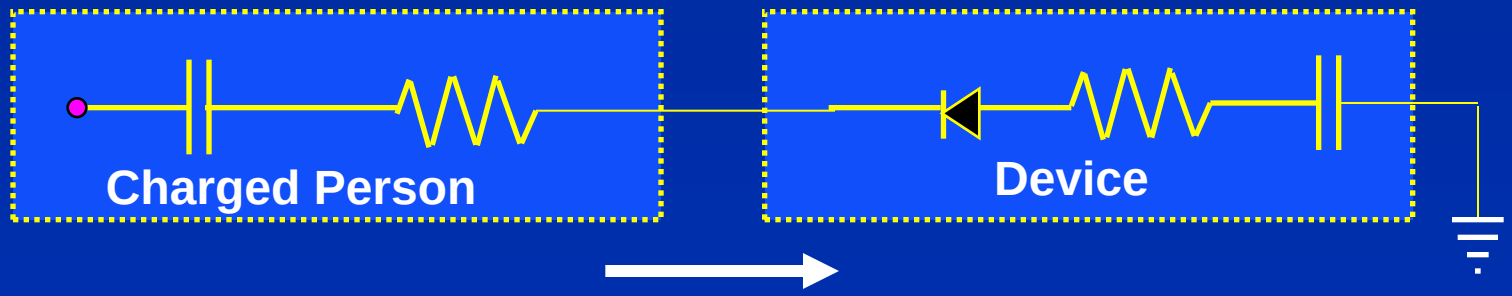
Human Body Model





When the air breaks down between the human's finger and an IC pin, charge is suddenly transferred from the person via the grounded pin of the IC to ground.



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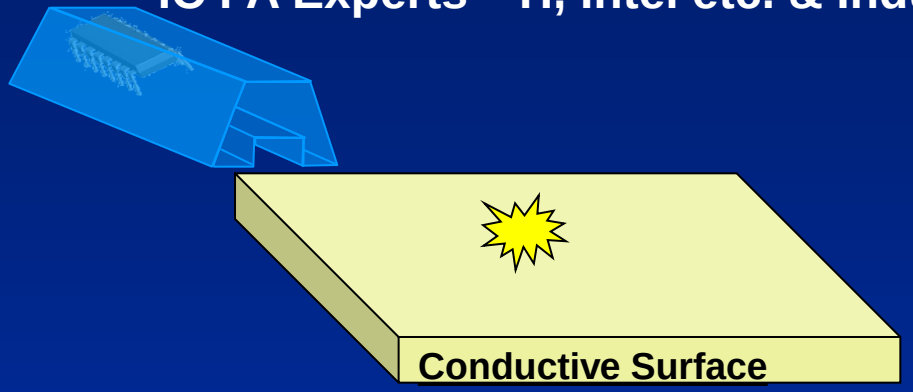
Charged Device Model

"99.9% of ESD Failures are CDM!"

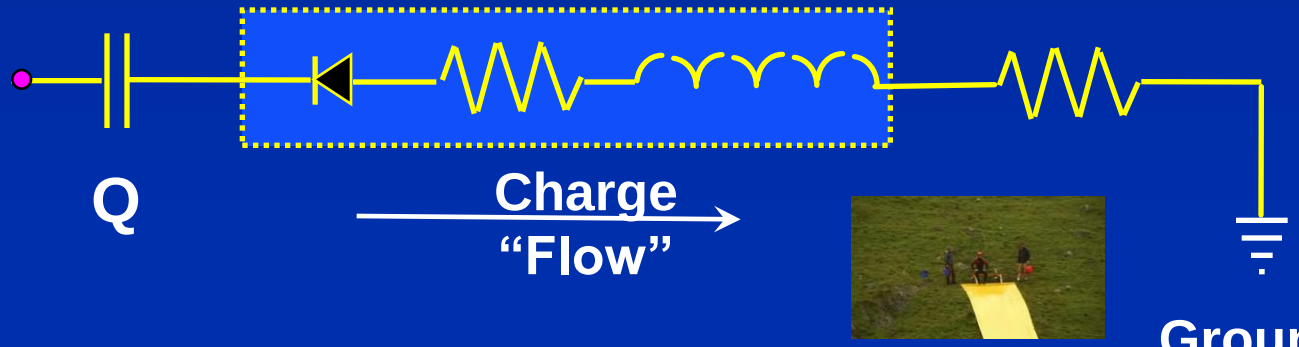
Andrew Olney, Analog Devices, Quality Director

IC FA Experts - TI, Intel etc. & Industry Council



Capacitance of Device

Contact Resistance



CDM Video

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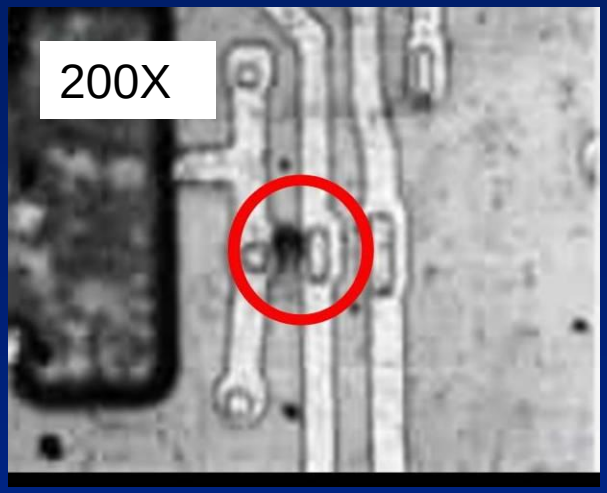
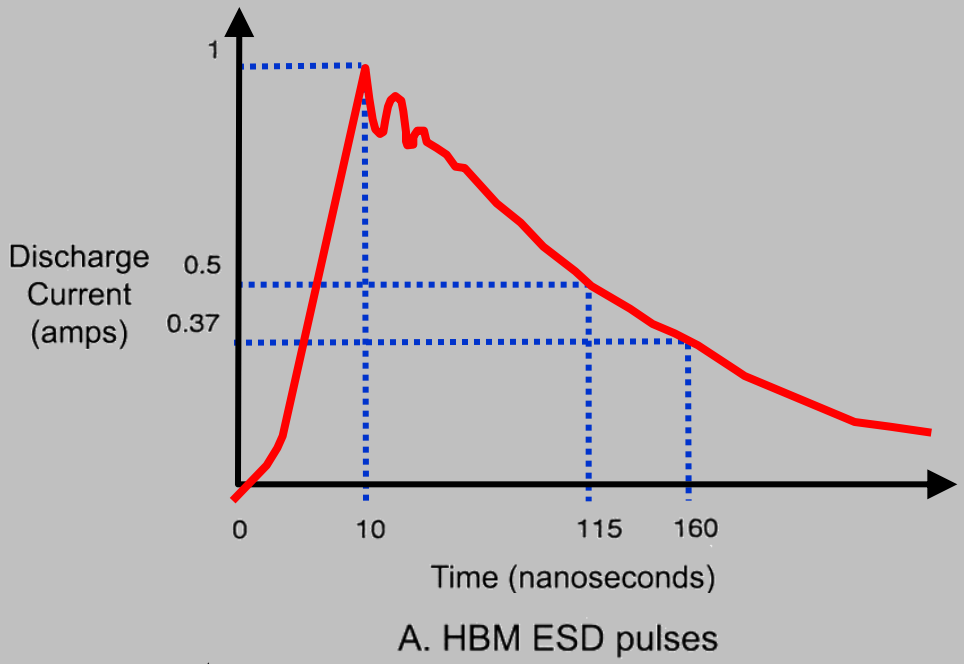
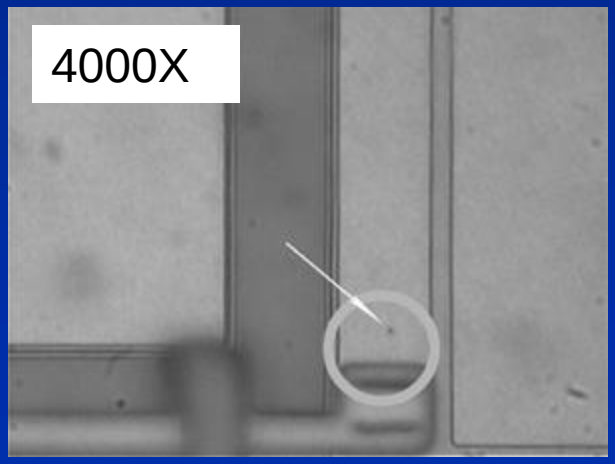
HBM

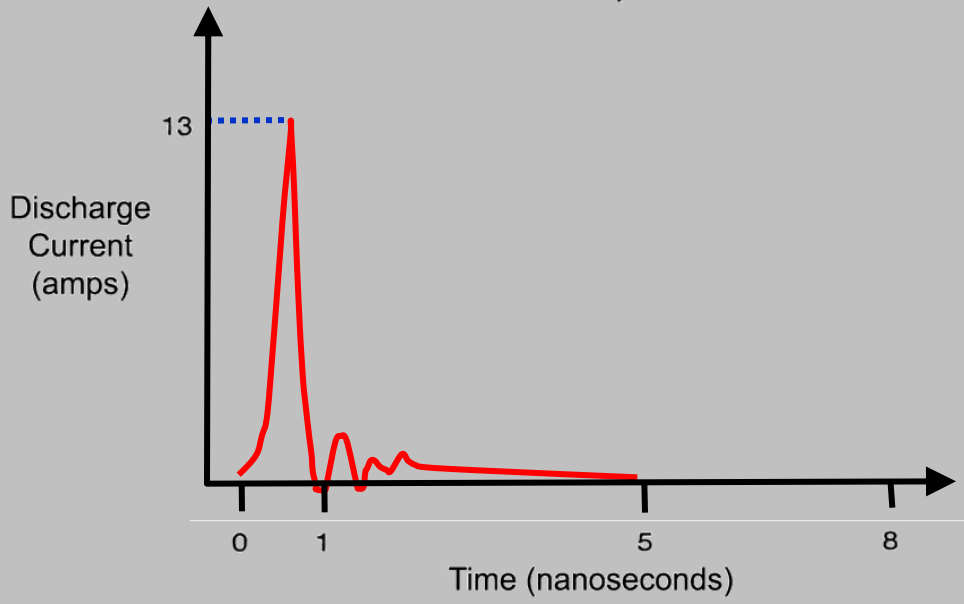




A. HBM ESD pulses

CDM





B. CDM ESD pulses

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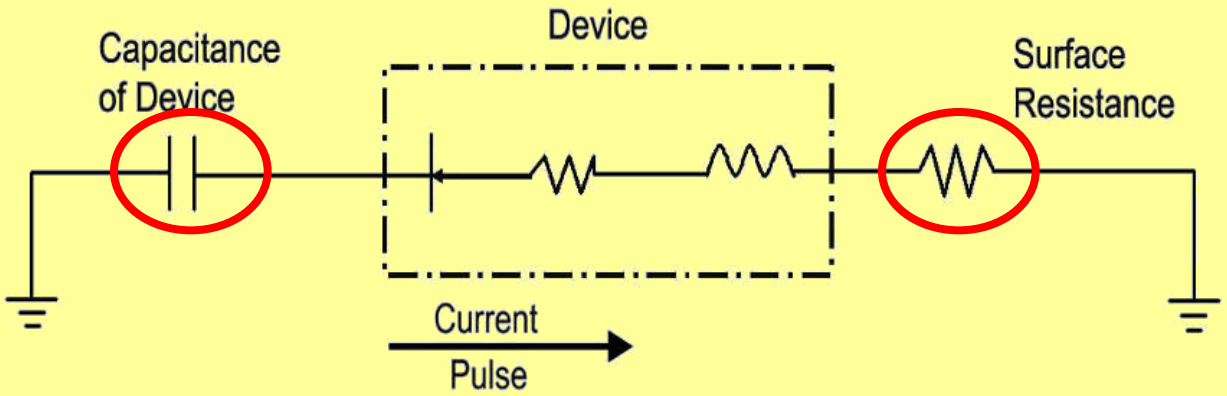
CDM & CBE Mitigation Best Practices

Two Strategies ⟵ Which One is S20.20?



Lower device voltage or higher surface resistance in the discharge path can *reduce discharge current*.

e.g. Charged Insulators

e.g. SRM Requirements

DA Recommendation: Add SRM requirements for Dissipative Materials at Point of Contact

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HBM vs. CDM FA Laboratory Failure Rates

- Vast Majority of ESD Failures are CDM In Nature
  - Includes: CBE, CDE, and Metal to Metal Discharges
  - Major IC Supplier FA Labs
  - Industry Council on ESD Target Levels
- ADI Has not Seen an HBM Failure in Over 3 Years
  - 99.9% of ESD Failures are CDM in Nature

  Ref: Andrew Olney, Analog Devices, Quality Director

Note: S20.20 HBM controls are an essential prerequisite for CDM/CBE/CDE controls. Without HBM controls in place CDM mitigation is virtually impossible.

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Myth #3:
Circuit Boards Are Less Sensitive To ESD Than Devices

Truth:
Exposed Circuit Boards are MORE Sensitive Than Devices Due to the Much Stronger Discharge Currents (up to 25 amps) of the CBE – Charged Board Event

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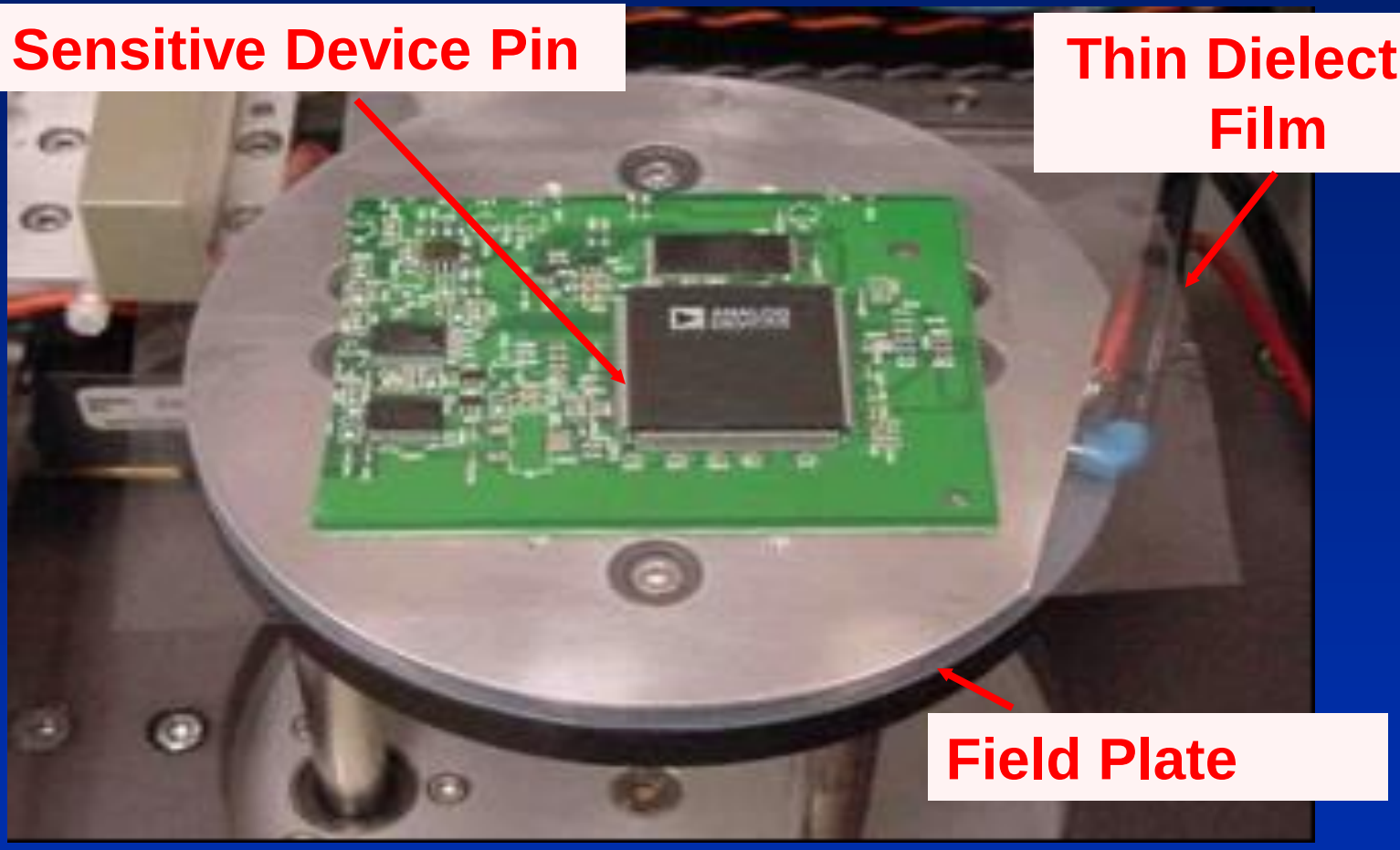
CBE Test Set-Up



CBE Test Method Setup For A Board

Olney et al (Analog Devices)

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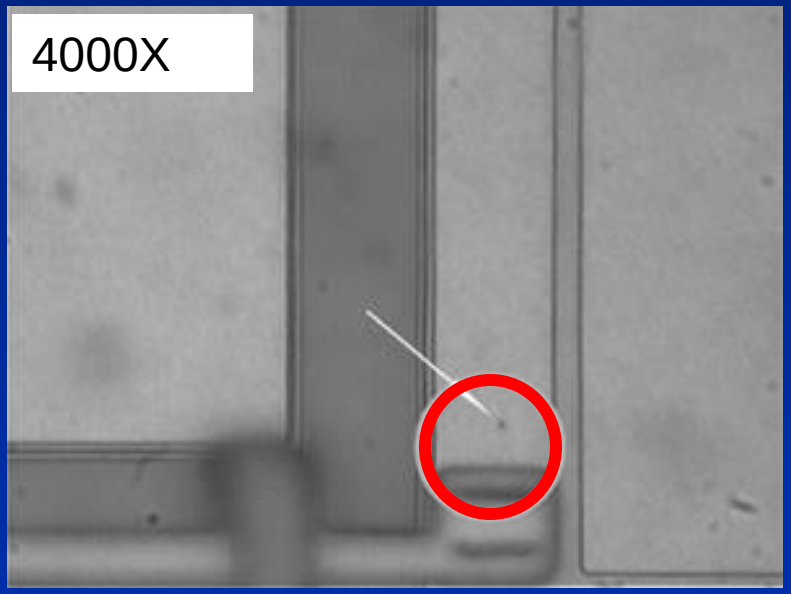
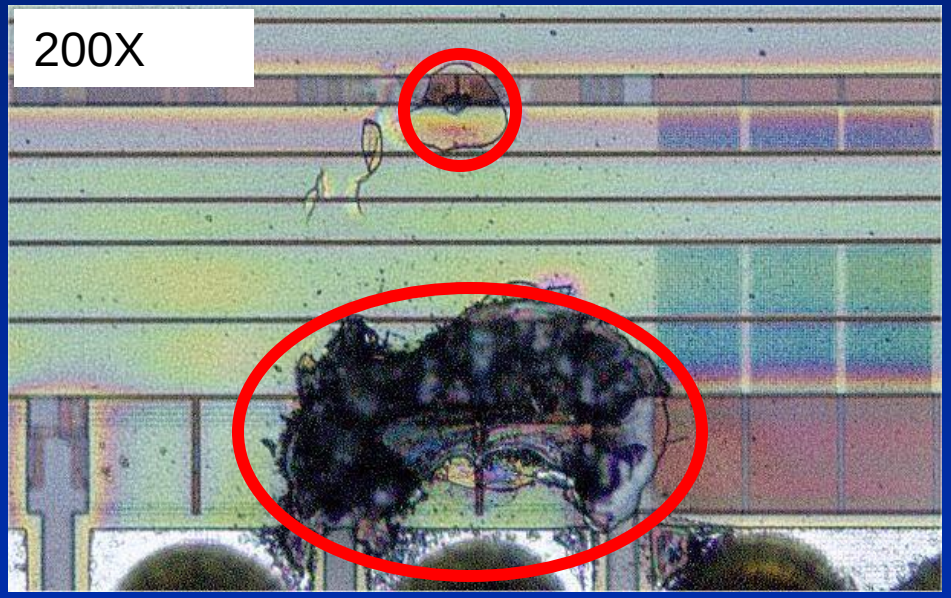
CBE ESD Damage - *A New Discovery!*
Most FA Experts Misdiagnose as EOS!!!!

Up to 50% of EOS Failures are CBE ESD! (2008)



CDM Device Damage



CBE (ESD)
Device Damage on Circuit Board

Courtesy: Andrew Olney, Quality Director, Analog Devices

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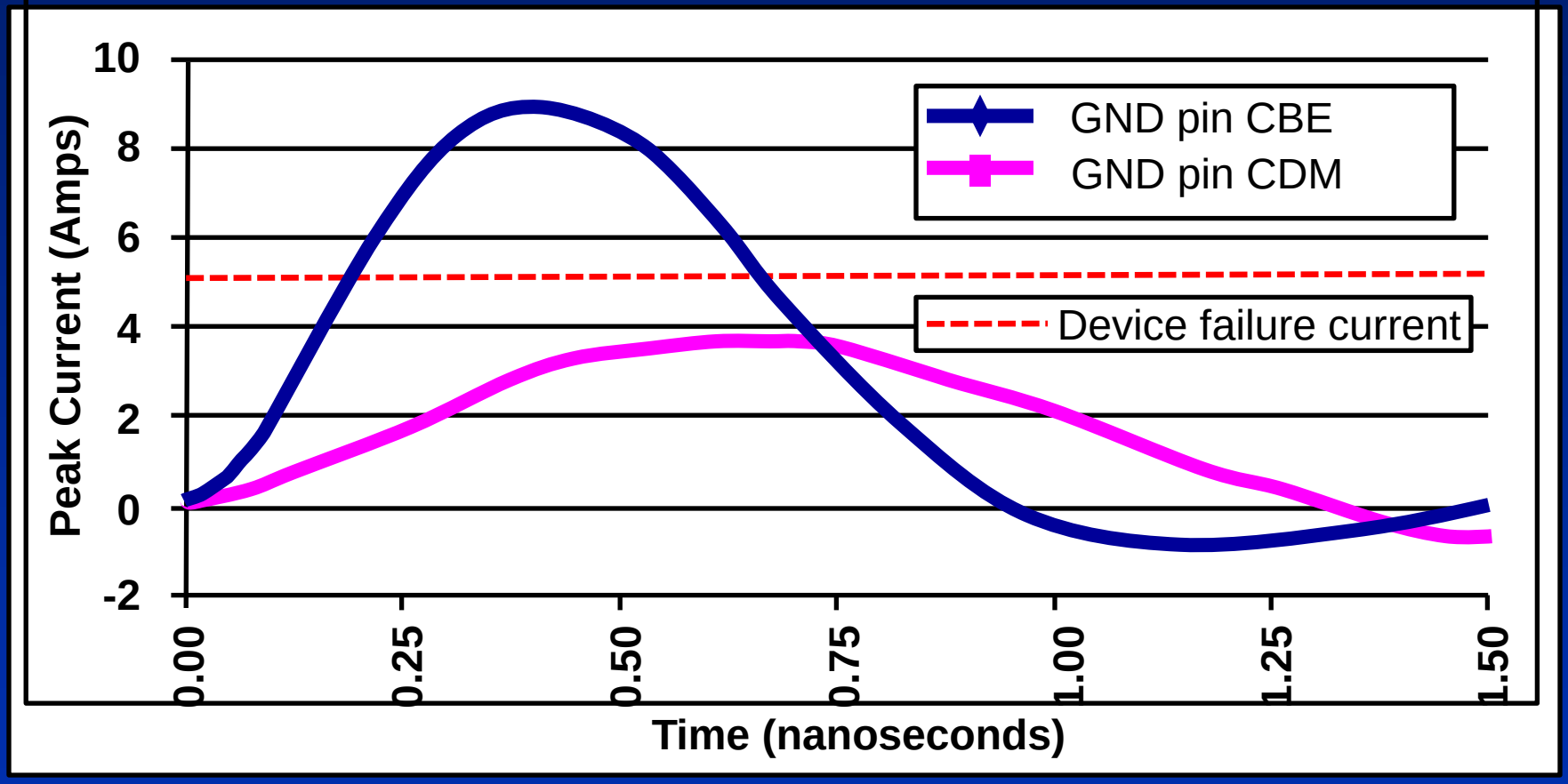
CBE vs. CDM Discharge Waveform Comparison (250 V)



Peak Currents of 25 amps Have Been Measured!

Courtesy: Andrew Olney, Quality Director, Analog Devices

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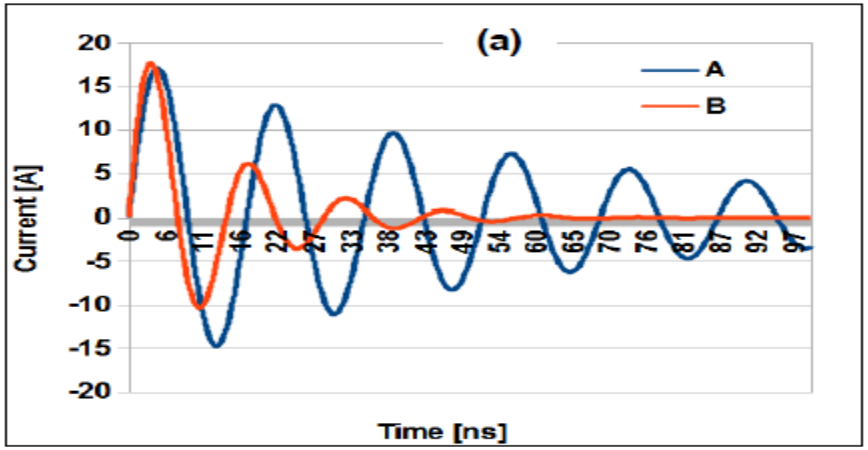
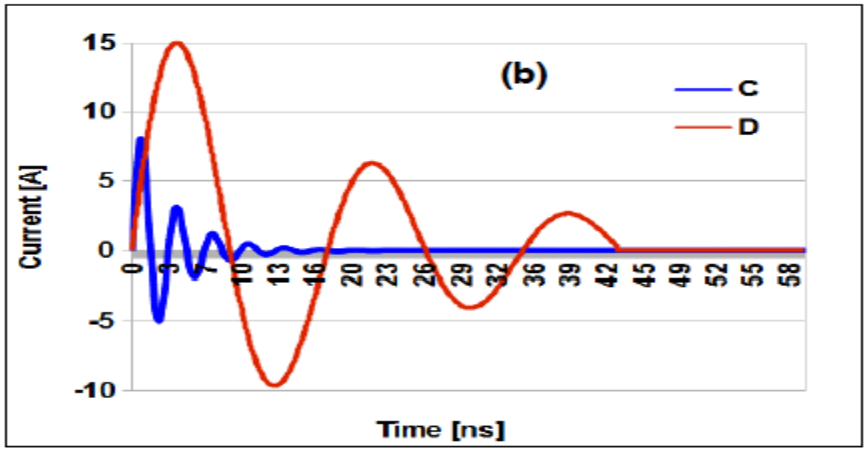
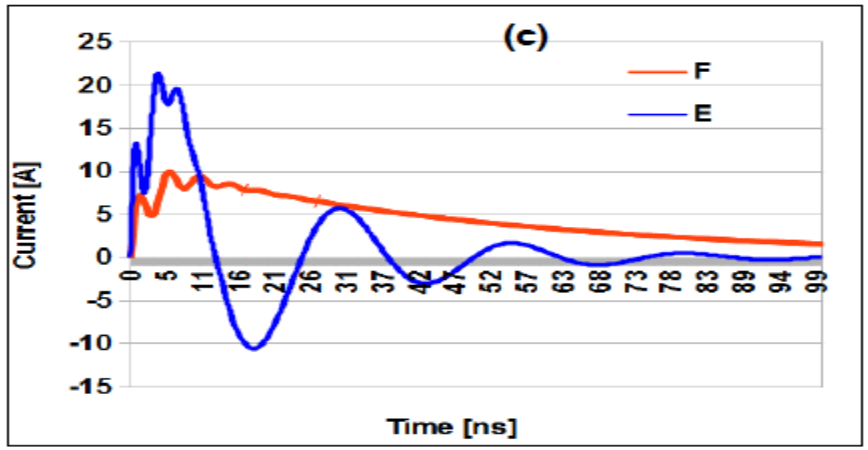
Variation in CBE Waveforms

A - High L, C
B - Lower L, C; higher R
C - Faster discharge (small C)
D - Slower discharge (large C)
E - Two RLC sources
F - High L, R







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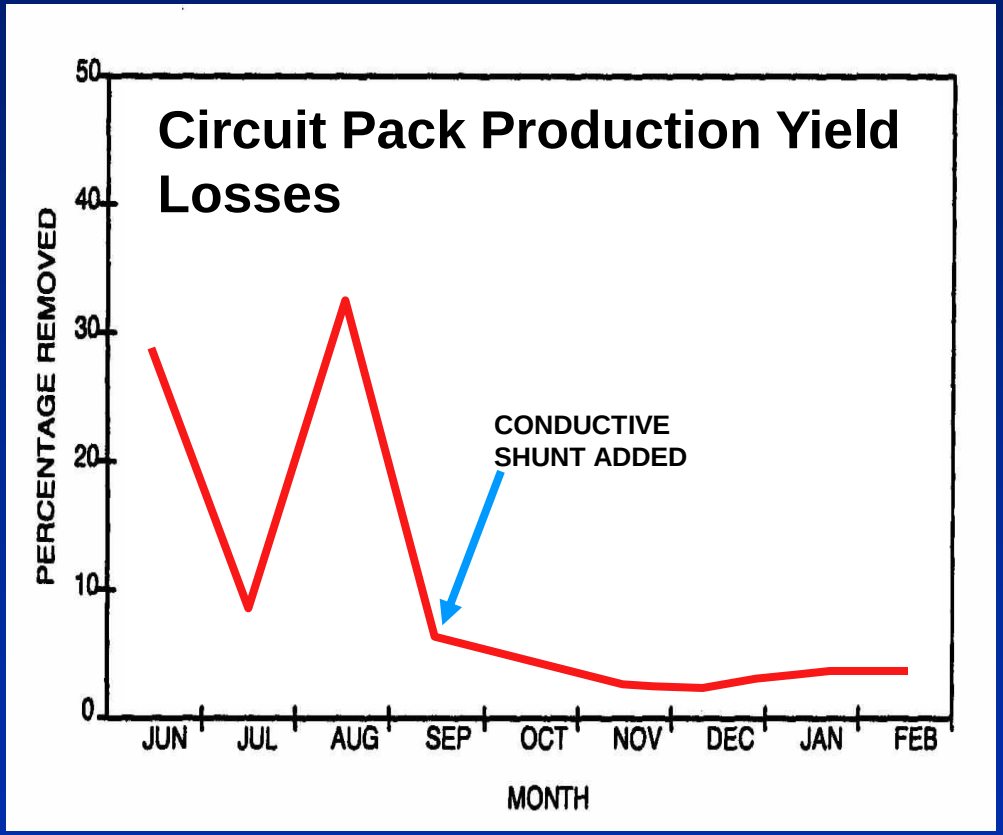
Customized Solutions Are Essential

Circuit Board - Class 000 Case Study:

- Design Transfer
  - No ESD Data
- 15 Volt CDM Threshold
- 100% Failure Rate: Some Lots
- $1.2B Sales Jeopardy
- $1K Invested in Shunt
- $6.2M/yr Savings Documented



Book: ESD PROGRAM MANAGEMENT
Ted Dangelmayer

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Steps Taken To Resolve Yield Losses

Cost of Implementation = $335,000

(That Did Not Work!)

- Enhance ESD Training
- ESD Flooring & Footwear
- ESD Chairs, Garments, Carts
- Room Ionization & Bench Top Ionizers
- Constant Wrist Strap Monitors
- Daily SPC to Ensure Compliance to Procedure
- Dissipative Handling Materials & Containers

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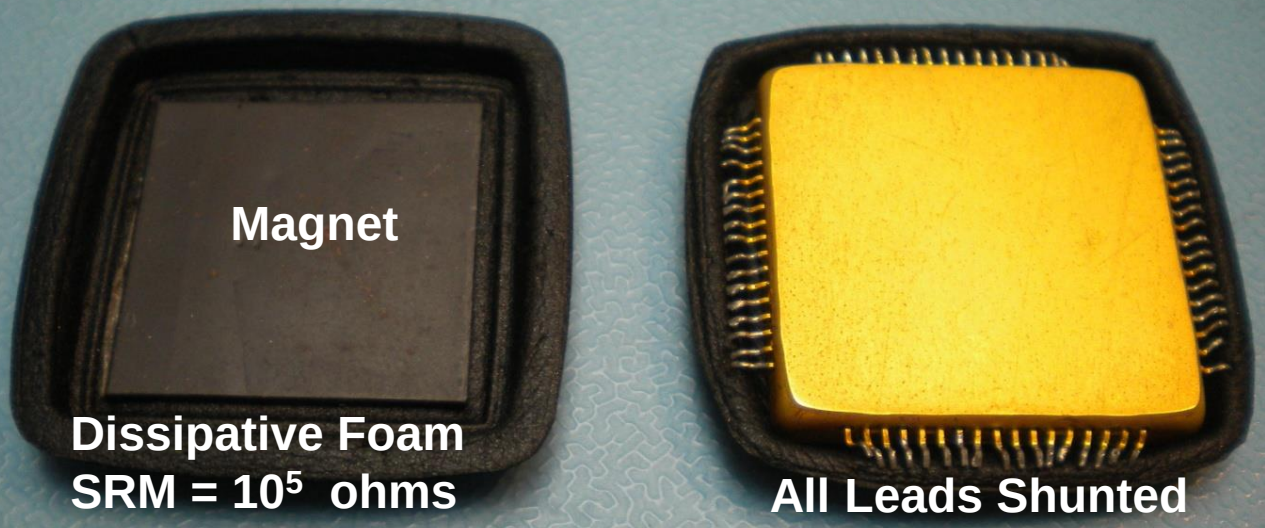
Customized Shunt Resolved Yield Losses – Class 000

Cost of Implementation (That did Work!) = $1,000

Placed Shunt on Device on Circuit Board After Solder Reflow

Withstand voltage = 15 Volts HBM & CDM



Dissipative Foam
SRM = 10^5 ohms

All Leads Shunted on Circuit Board

After Device Redesign:
Withstand Voltage = 750 volts – HBM
= 100 volts - CDM

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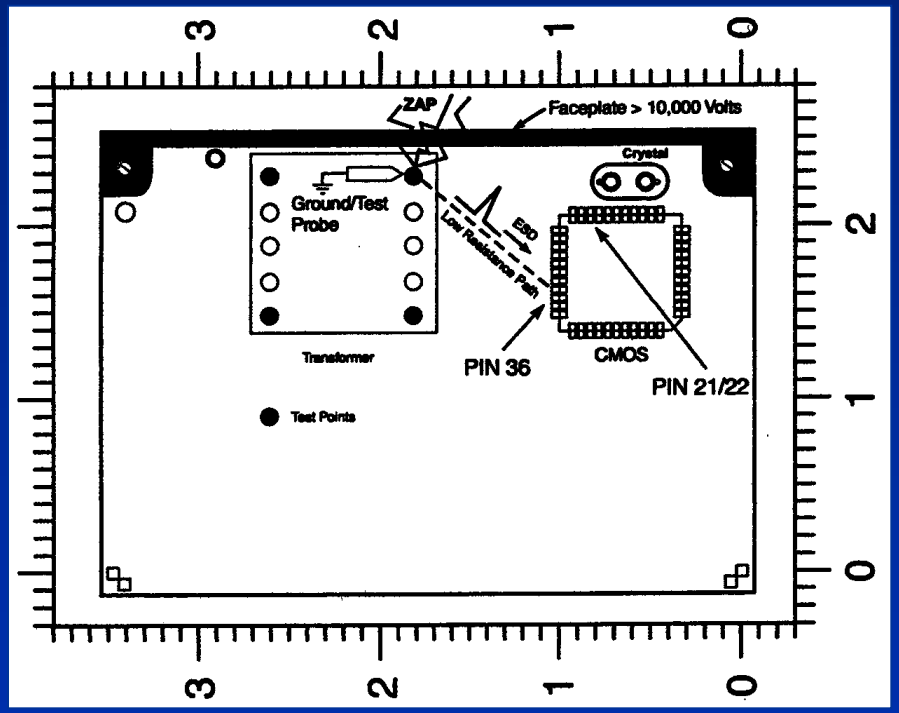
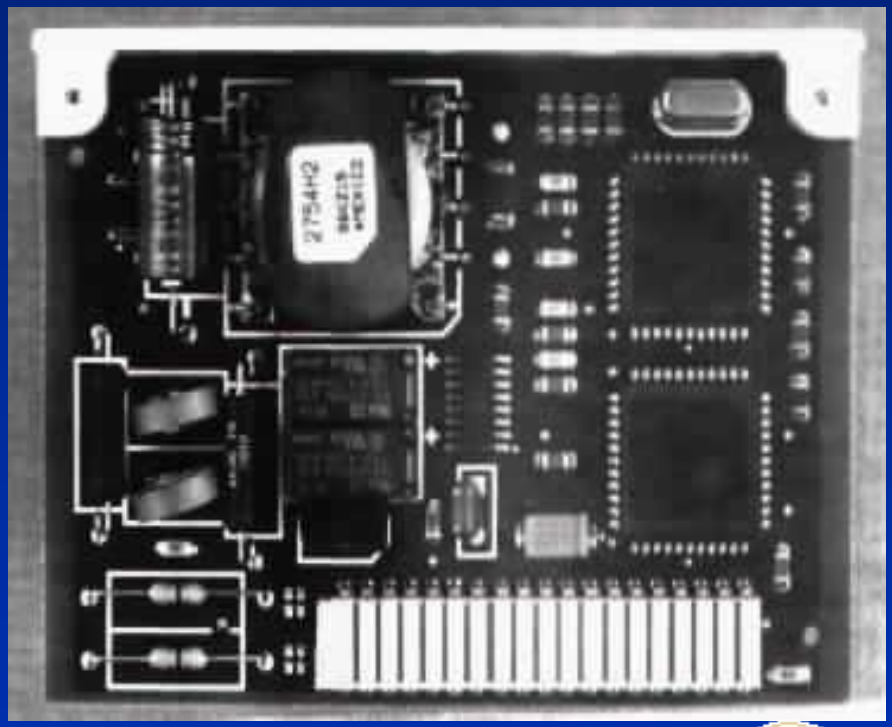
Faceplate Field-Induced CDM Failure

Established Code - New Faceplate Supplier

40% Failure Rate - 1.5KV CDM Threshold





Ref: ESD Program Management, 2nd edition, pp59-61

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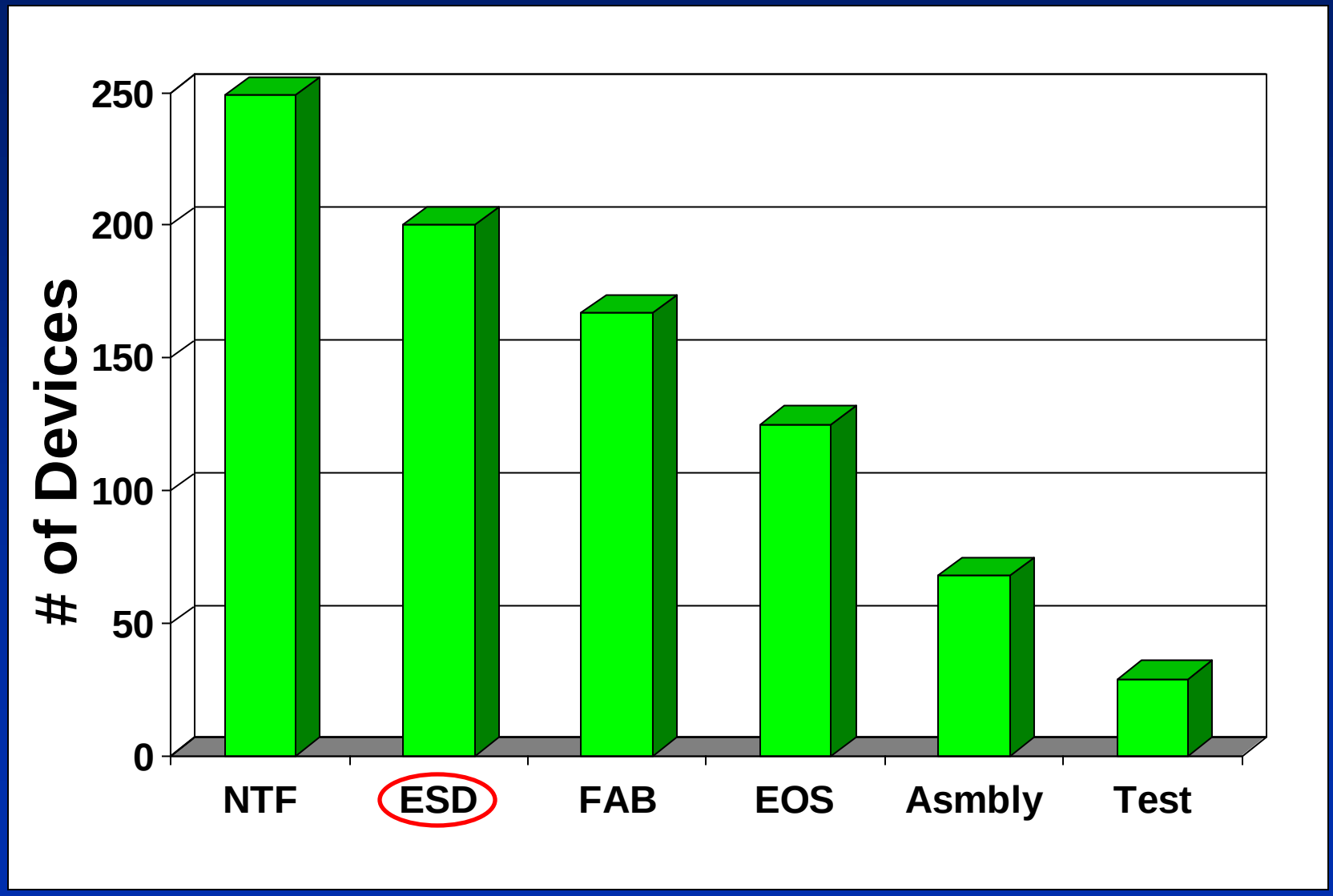
After Misdiagnosis Correction: ESD is #2 Cause of IC Failure!



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Myth #5:
Airflow Causes Charging

Truth:
Clean air flow does not charge or cause charging.

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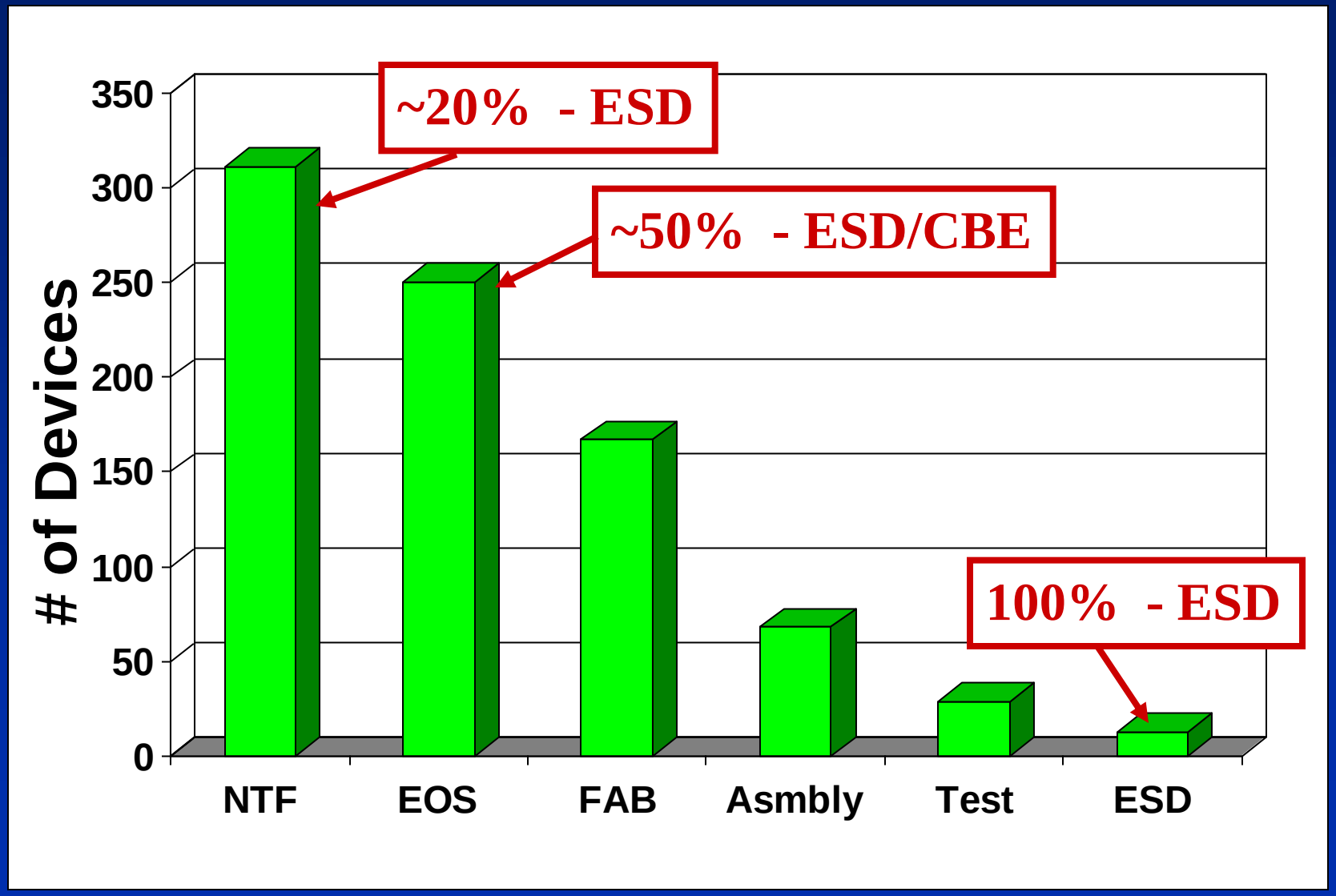
Typical IC Device Defect Analysis

What is Significance of CBE (ESD)?



Olney et al (Analog Devices)

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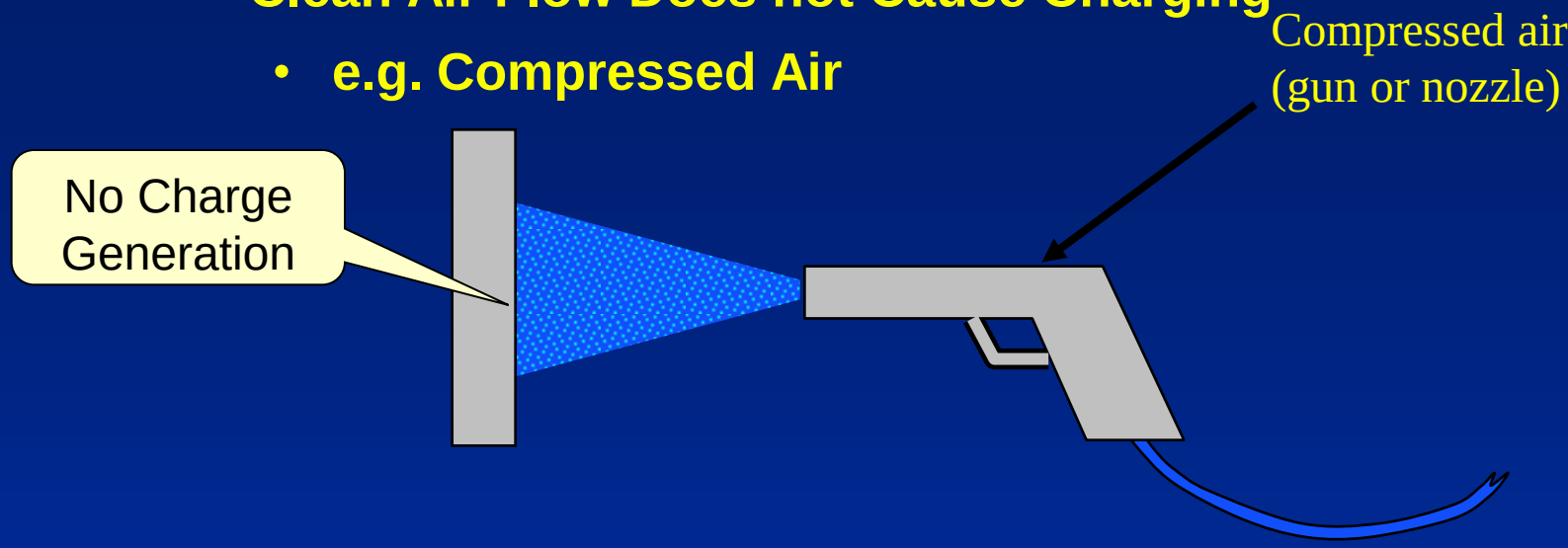
Does Air Flow Cause Charging?

- **Clean Air Flow Does not Cause Charging**
  - **e.g. Compressed Air**



- **Contaminated Air Can Produce Severe Charging**
  - **e.g. Sandblasting**

•Ref: Baumgartner, B, "The Misconceptions of Air Flow as a Tribocharging Source"' ESDA Proceedings, 1992

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Voltages Due to Air Flow Through Tubing

Air Flow Through Tubing			
Specimen Material	Air Tribocharge	Finger Tribocharge	2-Point Resistance
Polyethylene	< 10 V	400 V	> 10^{13} ohms
Rubber	< 10 V	150 V	4 x 10^{12} ohms
Polystyrene	< 10 V	200 V	> 10^{13} ohms
Polypropylene	< 10 V	500 V	> 10^{13} ohms

•Ref: Baumgartner, B, "The Misconceptions of Air Flow as a Tribocharging Source"' ESDA Proceedings, 1992

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Voltages Due to Air Flow on Surfaces

Air Flow or Action			
Specimen Material	Fan	Air Gun	Finger
Aluminum	< 10 V	< 10 V	< 10 V
Epoxy Fiberglass	< 10 V	< 10 V	+ 200 V
Conformal Coat	< 10 V	< 10 V	+ 210 V
Teflon	< 10 V	< 10 V	> - 2.5 KV

•Ref: Baumgartner, B, "The Misconceptions of Air Flow as a Tribocharging Source"' ESDA Proceedings, 1992

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Myth #6:
Metalized Shielding Layers Are Essential

Truth:
Dissipative materials combined with air gaps provide ample protection for the vast majority of applications. Electronic Devices Seldom Require Metalized Shielding.

Exceptions: Reticles, SAW filters and other components with very small air gaps require metalized shielding.

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Dissipative vs. Shielding Considerations

- Dissipative materials are essential for Intimate contact with Class 0 Devices!
- Devices that fail simply in the presence of a field are extremely rare.
  - Real world circuit designs minimize path lengths to satisfy EMI susceptibility requirements. As a result, field gradients on boards and devices are not sufficient to cause current transients strong enough to damage even Class 000 devices.
  - 3M Demo Example - MOSFET & Styrofoam Cup
    - Special circumstances are necessary to produce field gradients locally strong enough to cause a device to fail.
- Electrostatic fields can be dealt with by using air gaps. (Ref Fowler Paper – EOS/ESD Symposium)

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Dissipative vs. Shielding Considerations

- Arcing directly through a static dissipative bag without shielding is unlikely below 5,000 volts.
- 1/2 inch air gaps provide 25,000 volts arc through protection
- Published studies on shielding effectiveness often involve extreme worst-case scenarios
- Sound Global ESD programs have been very successful without the use of shielding materials

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Device Damage Thresholds Inside Various ESD Bag Types*

Test Method:
ESD simulator discharged to outside of bags with 200 volt HBM device inside

Material	Damage Threshold Voltage (V)	
	New Bags	Used Bags*
Insulative Bag	4,000	
Antistatic (pink poly) Bag	4,500	
Static Dissipative Bag	5,000-6,000	
Low Charging Bubble Wrap	4,500-6,500	6,000
Low Charging Foam Wrap	>6,500	
Shielding Bags (3 types)	6,500-8,000	5,000-6,000
* New bags were crimped or folded once to simulate use.		

Ref: ESD PROGRAM MANAGEMENT by Ted Dangelmayer, second edition, page 369

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Air Gap Discharge Shielding

- **Rigid Dissipative Packaging Can Provide Shielding from ESD events**
- **1/8” gap protects Class 0 devices from IEC HBM discharges up to 35kV**

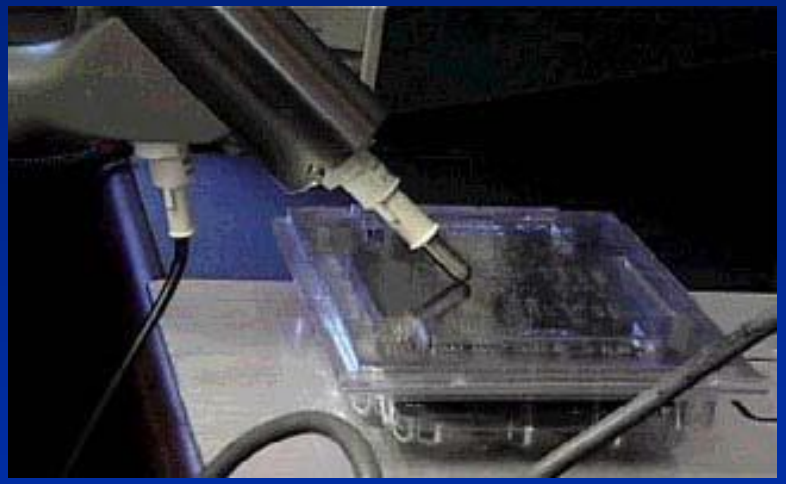

Photo courtesy of Fowler Associates and ESD Journal

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Myth #7:
MM Is A Valid Simulation Related To Machines

Truth:
MM has been downgraded by 3 standards bodies ESDA, JEITA, & JEDEC and is no longer required for JEDEC device qualification.

CDM is the Best Simulation for device discharges with charged or uncharged metal surfaces.

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MM Down Graded: JEDEC & JEITA & ESDA

- Test Results Do Not Match Real World Failure Modes
  - ADI FA Has Never Found a MM Failure
- No Work Was Done To Replicate Real World Damage
- The Title Machine Model Is A Misnomer
  - Does Not Relate To Machines
  - Developed As A Low Voltage Human Body Model
- Thresholds Correlate Well With HBM (~ 1/7 To 1/10 Of HBM)
- The Discharging Current Waveform With Metal To Metal Contact Similar To CDM
- No Longer Required by JEDEC for Device Qualification

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Myth #8:
Humidity Control is Essential for ESD

Truth:
Strategic use of static dissipative materials and ionization is both more effective and less costly.

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Typical Electrostatic Voltages vs. Humidity

Event	10%	40%	55%
Walking across a carpet	35,000	15,000	7,500
Walking across a vinyl floor	12,000	5,000	3,000
Walking across a Rubber Floor	800	600	200
Motion of Bench Employee	6,000	800	400
Removing DIP's from Plastic Tubes	2,000	700	400
Removing DIP's from Foam	14,500	5,000	3,500
Removing PWB's from bubble Wrap	26,000	20,000	7,000
Egg Crate Low Density Foam	21,000	11,000	5,500

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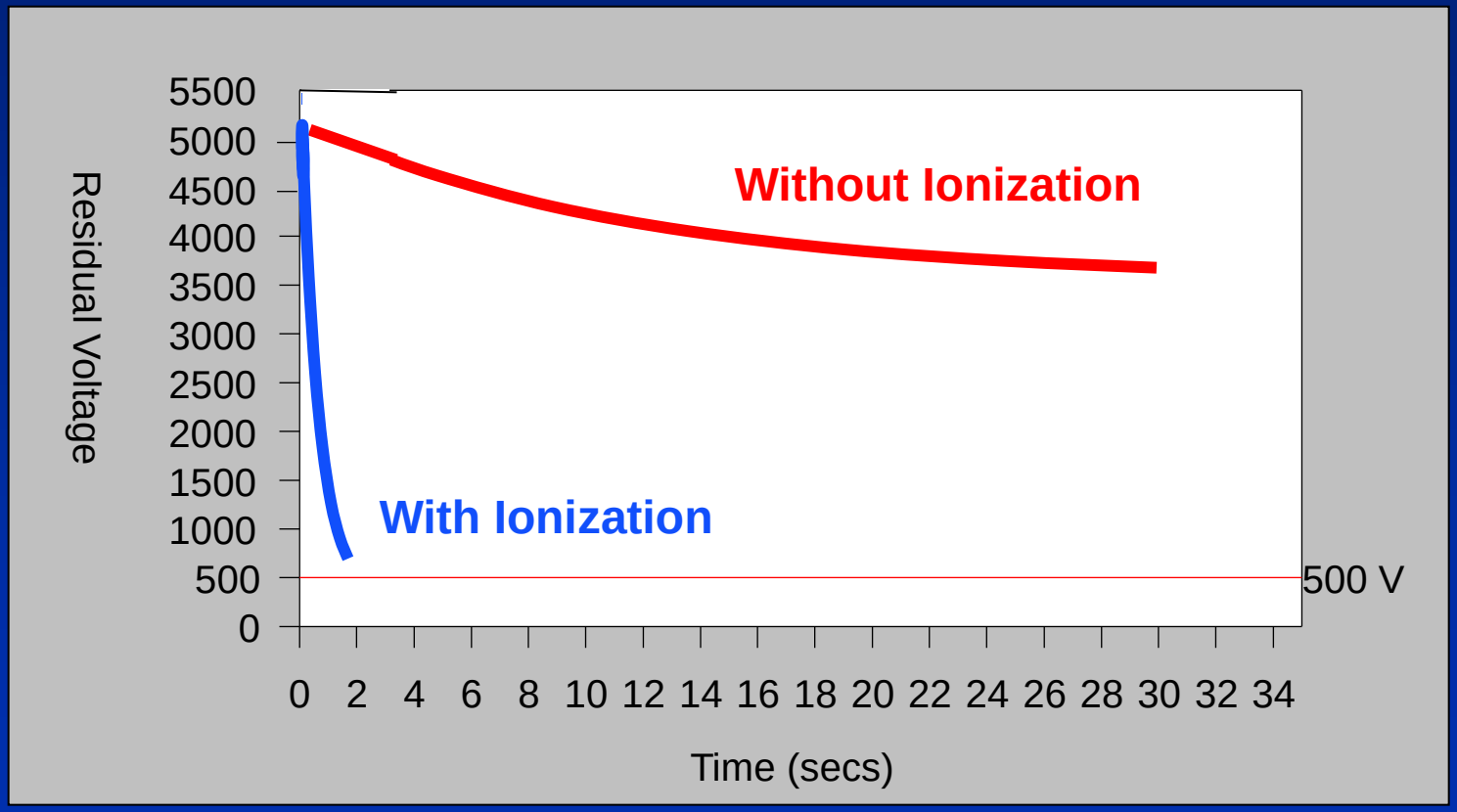
Static Neutralization: With And Without Ionization



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Ionizer Decay Times

Discharge Times 1000V to 100V	
Normal Air with 60% RH	>36,000 seconds
With Ionization in...	
Laminar Hood	10 - 20 seconds
Cleanroom	20 - 60 seconds
Air Conditioned Room	50 - 500 seconds
Workbench	2 - 20 seconds
Compressed Gas	0.1 - 5 seconds

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Case Studies – RH vs. Ionization

- Field Tracking Study - Florida
  - 55% RH – No Ionization
  - FA Results – 30% ESD Damage
- Central Office Test Set Damage
  - 50% Test Set Failure Rate
    - RH 45% - No Ionization
    - Distribution Wiring Continuity Test
    - Wire Installed 3 Months Before Test
- High Volume Manufacturing – Multiple Sites
  - 7% RH – Class 0 Devices
  - Strategic Ionization
  - 15 Year Period
    - HBM Failures = 0
    - CDM Failures = 3

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Myth #9:
Fieldmeters Make Accurate Measurements on Machines

Truth:
Most machines utilize metal in close proximity to the areas where field measurements are needed. These metal surfaces (0 volts when grounded properly) greatly lower fieldmeter readings because anything within the fieldmeter 4 inch field of view is averaged into the measurement.

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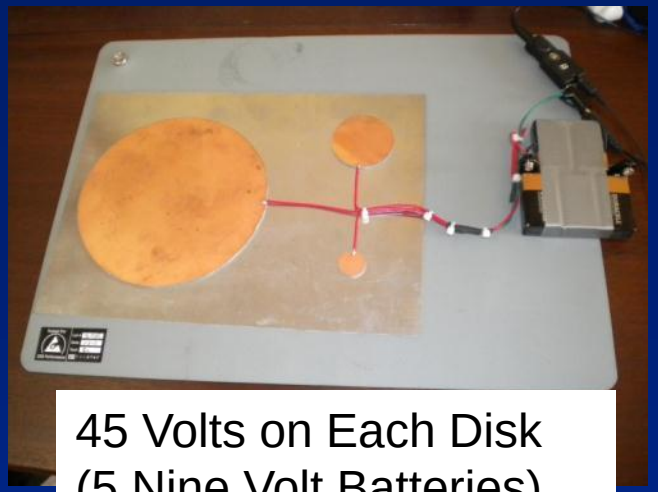
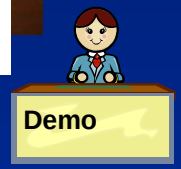
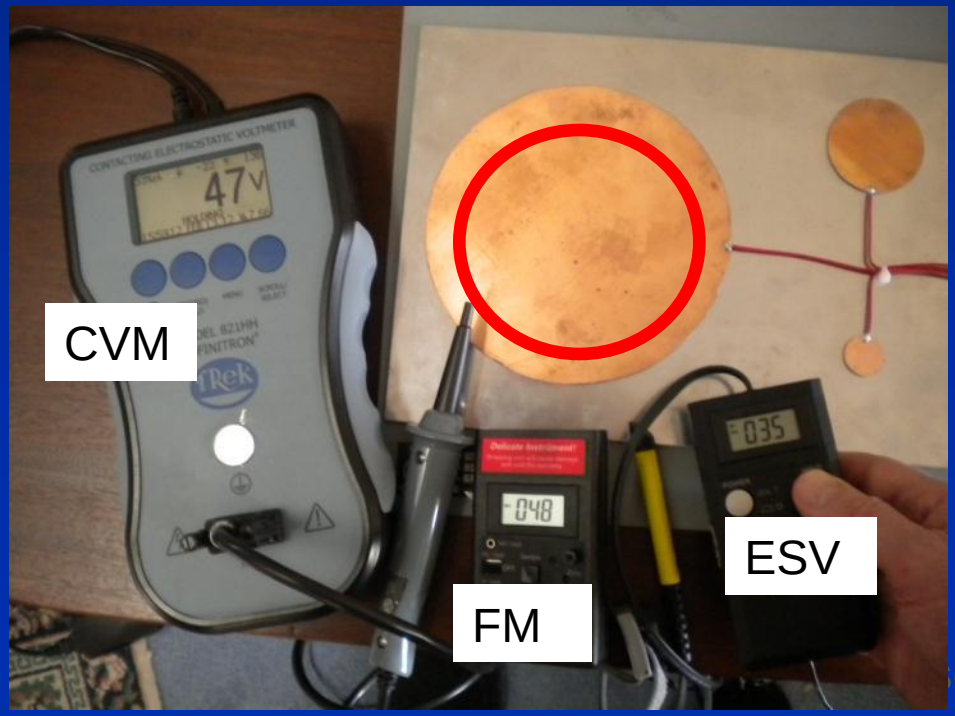
Voltage Measurement Comparison:

CVM Contact Voltmeter
ESV Electrostatic Voltmeter
FM Field meter



45 Volts on Each Disk
(5 Nine Volt Batteries)





Field Measurement = 500 volts/in. – Why?

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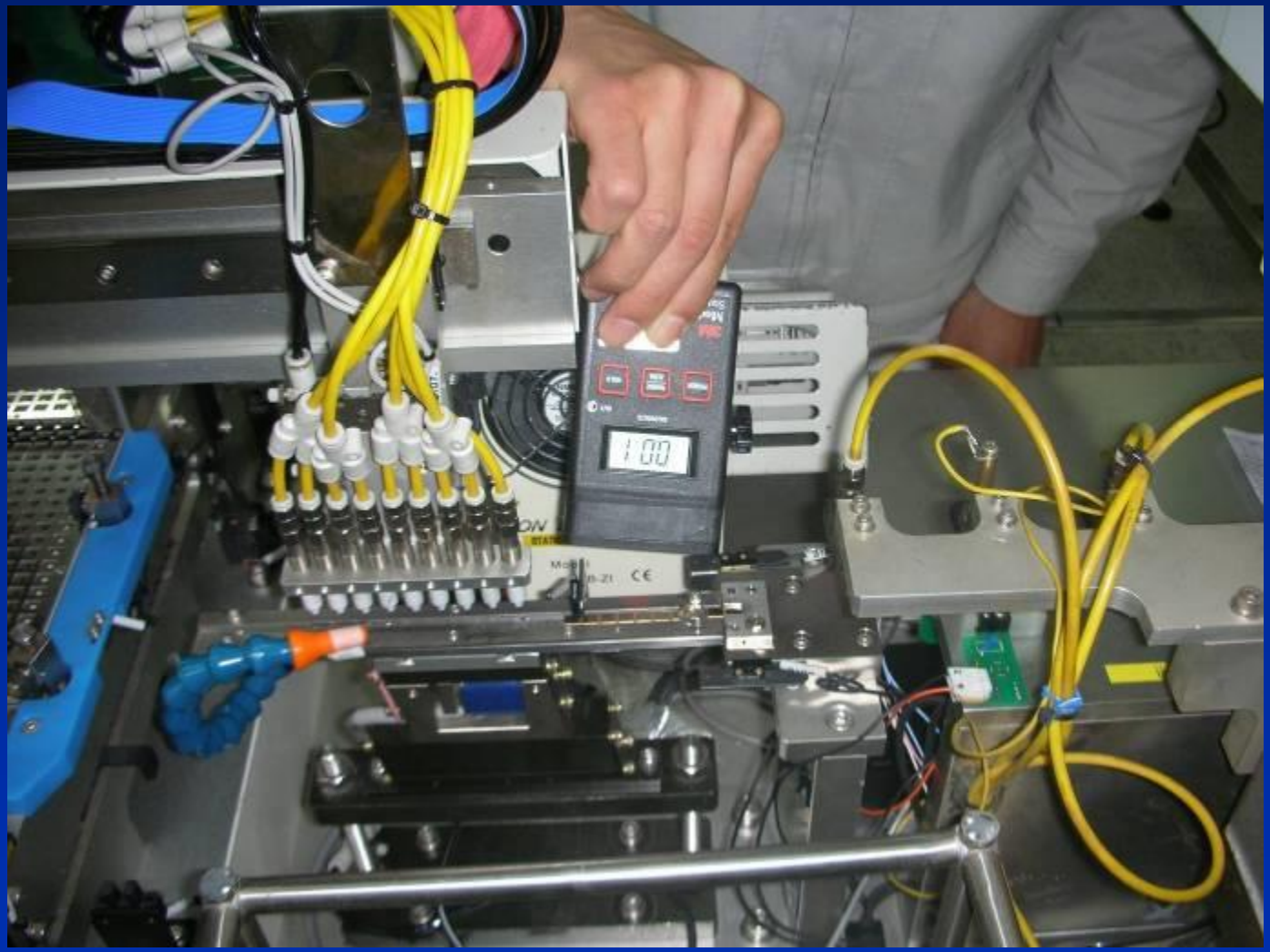
Grounds Lower Field Measurements



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Myth #10:
Ionization is Sufficient for Class 0 Applications

Truth:
Voltage controls are subject to human error. Even with ionization it is virtually impossible to continuously maintain voltages below the thresholds of extremely sensitive devices. This is especially true for thresholds below 50 volts.

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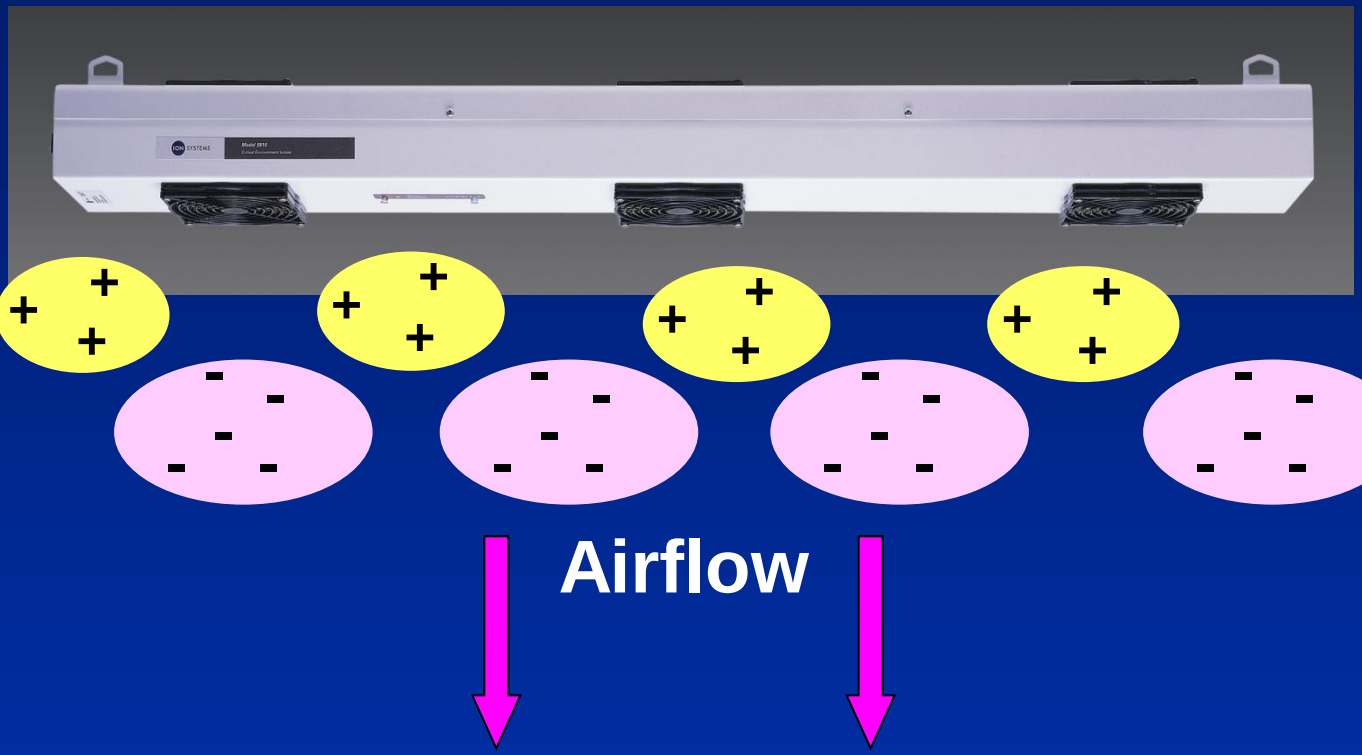
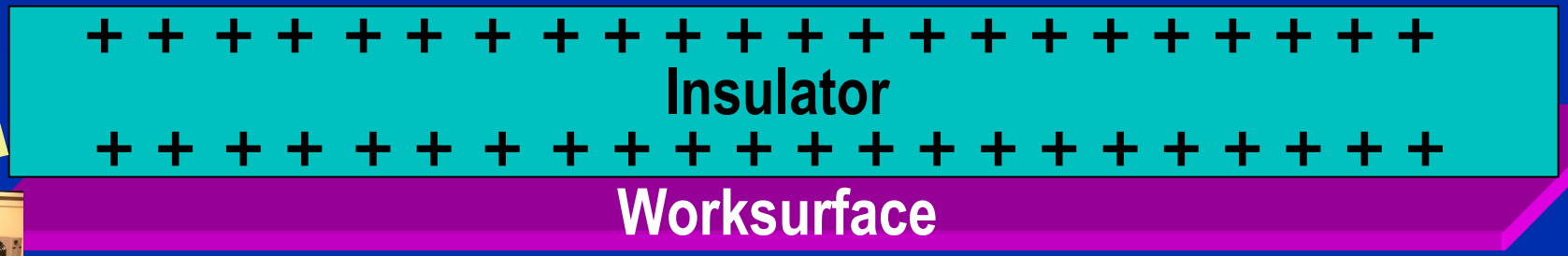
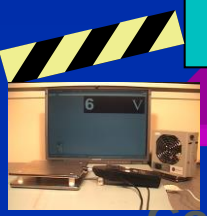
Ions Must Reach the Charged Surface







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How Well Can We Really Control V?

- **How Well Can We Really Control V Indirectly On A *Floating* Device/Tool?**

  - **~1000 V…all Of The Time**
  - **~100 V…….Some Of The Time**
  - **~10 V…….Hardly Ever**
  - **~1 V……..Never**

- **Voltage Controls Subject To Human Error!**

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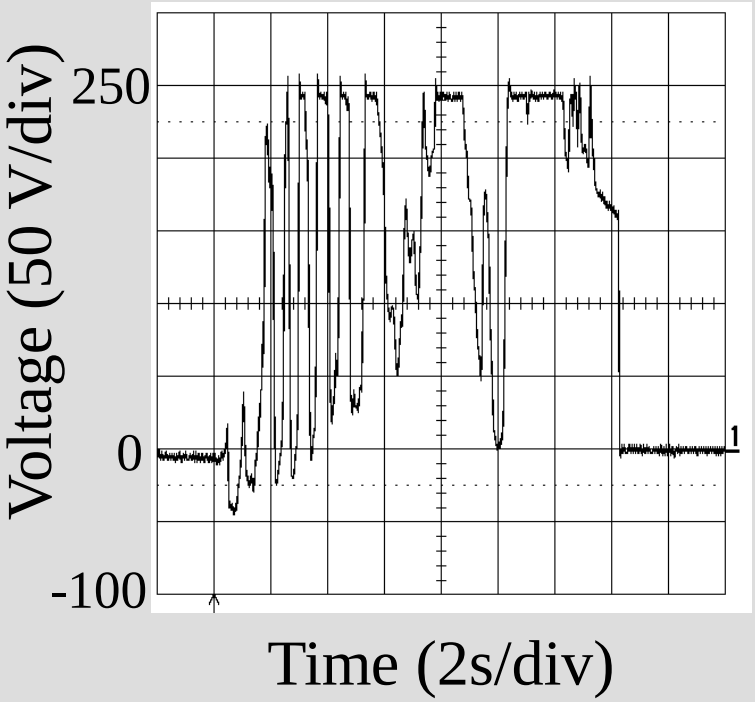
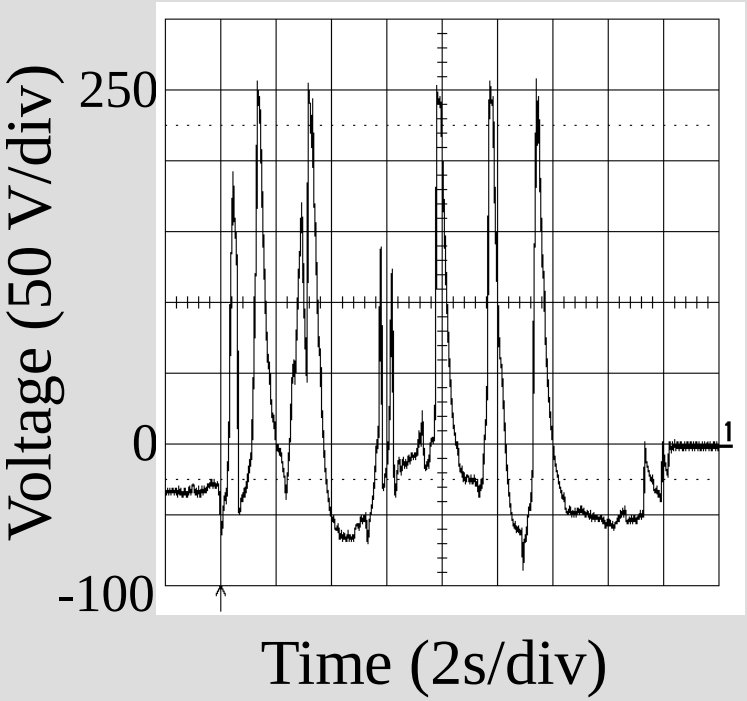
PCB + Nitrile Glove

Floating PCB handled with glove

No ionizer



With ionizer



- **Ionizer ON: Peak voltage still 250V!**
- **Don't depend on ionizers for Class 0 devices!**

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MR Head Lessons Learned

- Conventional ESD Methods ***Essential*** but ***Insufficient***!
  - Below 100 Volts
  - Ionization - Necessary but Insufficient
- Expect a Paradigm Shift @ 100 volts
  - Assume Device Still Charged!

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Will Ionization Work Here?

Not likely due to metal in close proximity to device

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Will Ionization Work Here?

Not likely due to metal in close proximity to device

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What is Wrong Here?

Ionizers are facing in wrong direction

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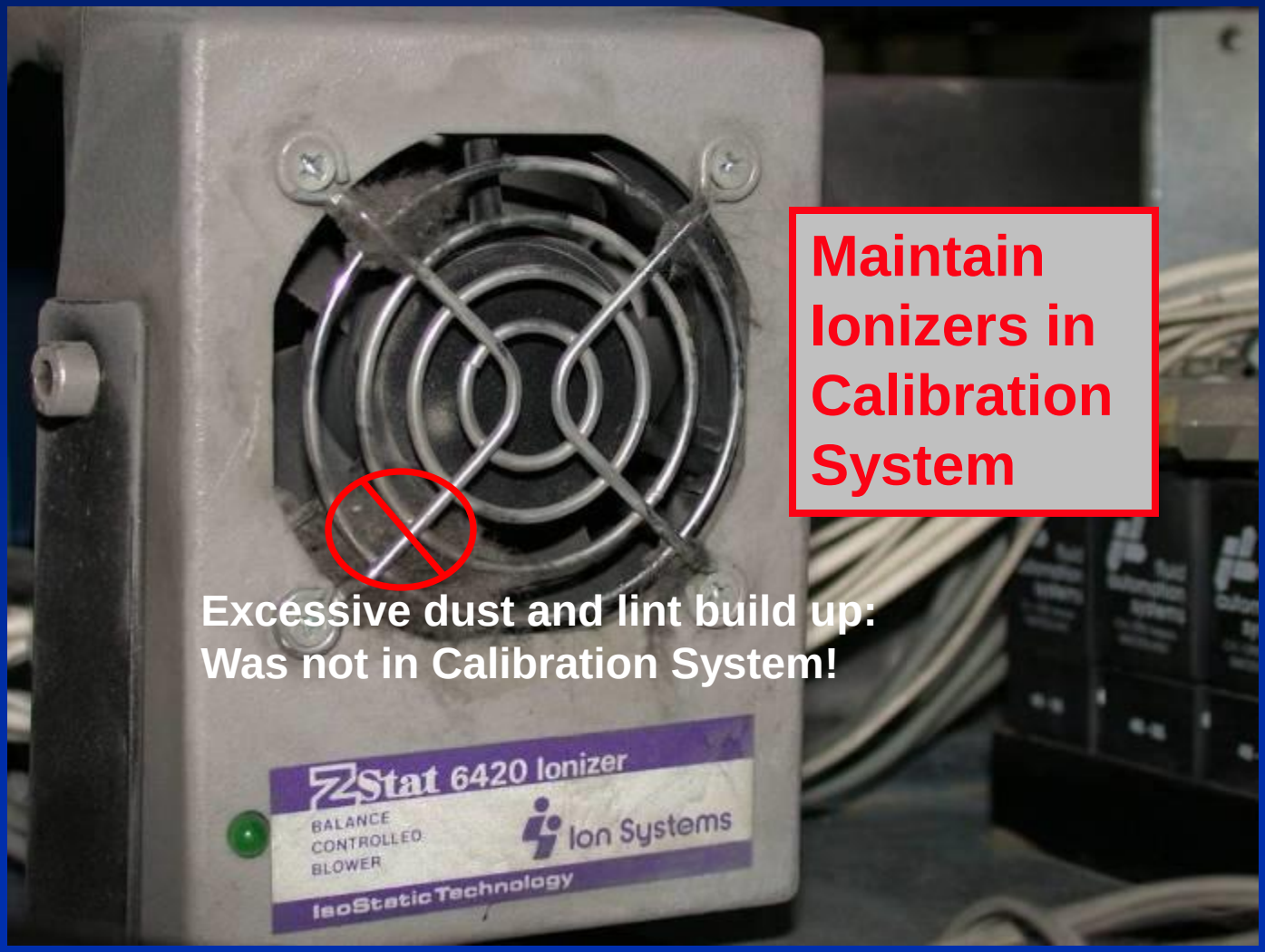
What is Wrong Here?



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Myth #11:
Latency Failures Comprise 90% of ESD Failures

Truth:
It is unlikely we will ever be able to accurately determine the extent of ESD latent failures but 90% is a gross overstatement. Latency does occur and some technologies such as Lasers and opto-electronic devices are more prone to latent failure.

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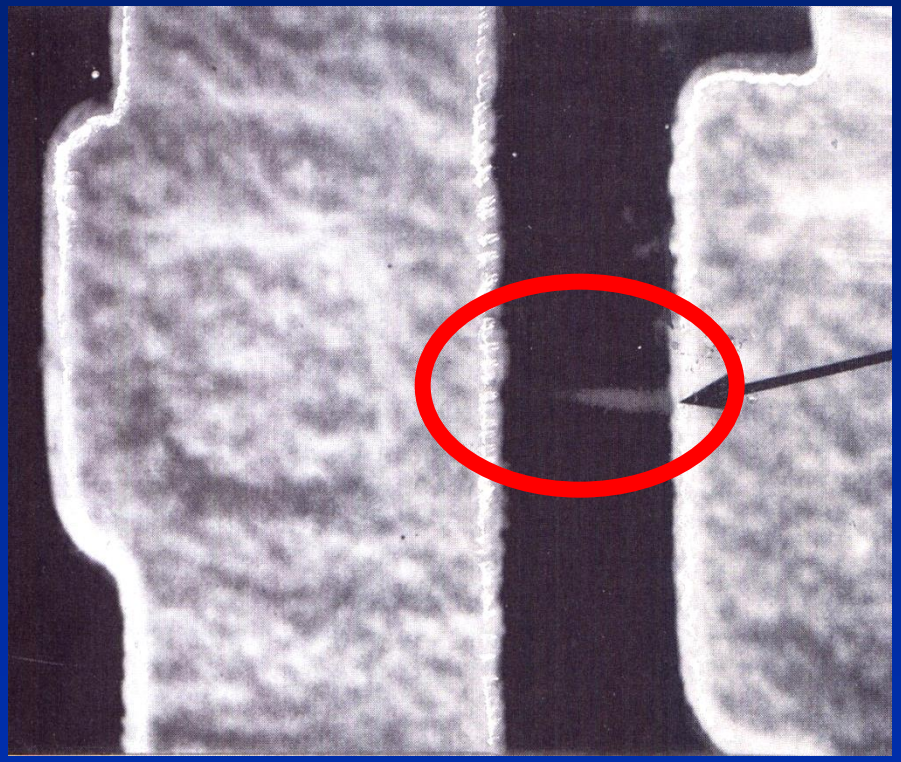
ESD Damage
A Quality & Reliability Issue

- Bipolar Junction
- 450 Volt HBM Withstand Voltage
- 3 of 15 Failed QA Tests
- 5 of 24 Circuit Boards Failed after Five Days
- Customer Failures: 17 of 31 Circuit Boards Failed after two Weeks

Latent Failure



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An Example: HBM Latency Risk for MOSFETS:

Generic MOSFETs do display latent effects of sub-threshold events.

- Literature studies show significant damage only when pulses are within about 5-10% of the threshold (See Tunnicliffe et al J. Electrostatics 1993)
- Even then multiple pulses are typically required to produce the latent damage sites
- Normal HBM ESD precautions typically keep voltages well under 5 volts
- Excursions from normal are *highly unlikely* to produce damage in the latency region without also causing catastrophic damage to some parts.
- Thus, latency risk should track HBM ESD dropout risk
  - If no HBM ESD failures have been observed it is highly likely that no latent damage has occurred as well
  - If HBM failures have been observed, the risk of latency is the about the same regardless of which handling method is used.

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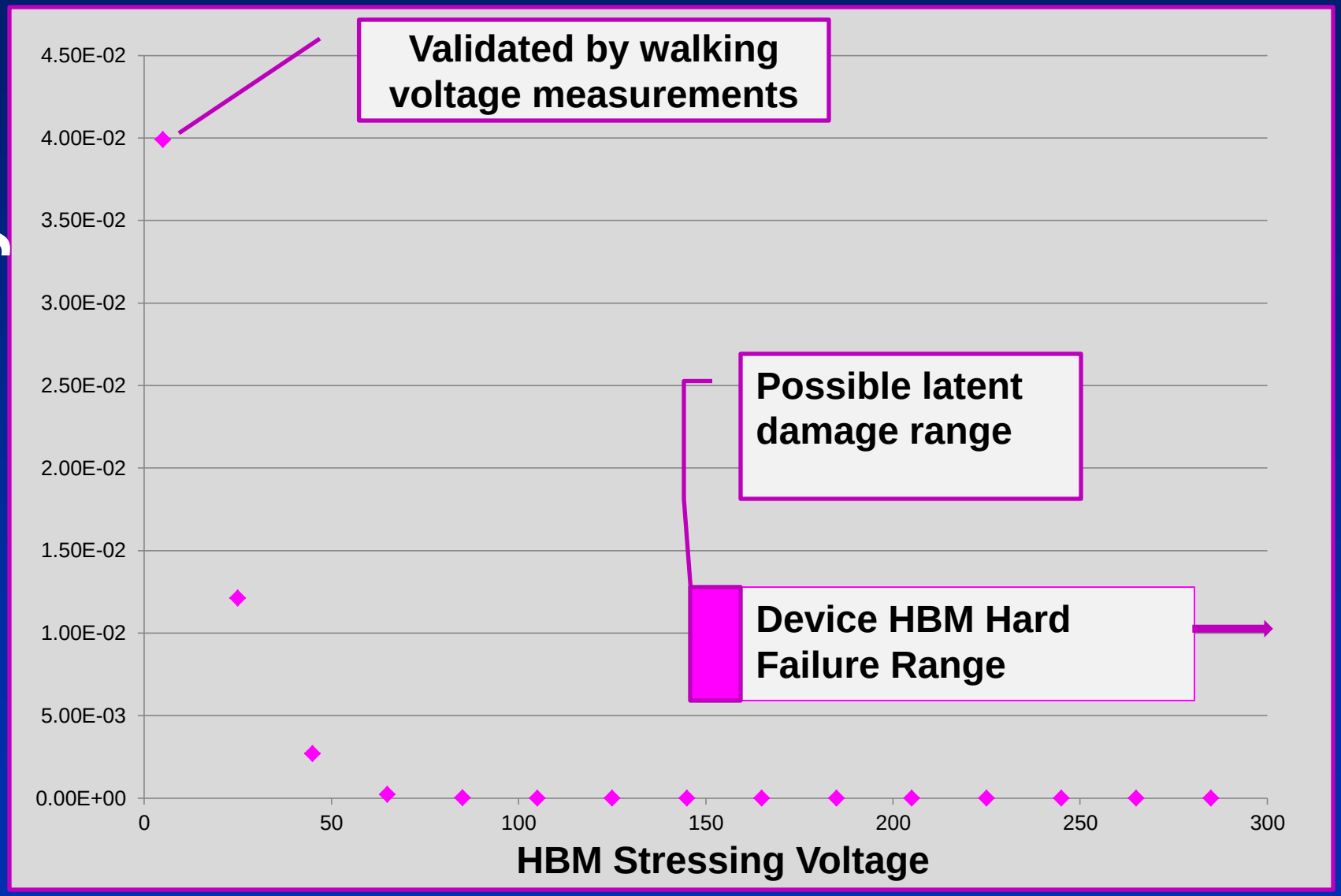
HBM Voltage Distribution with Basic S20.20 Controls in Place



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